IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl.No.:	09/918,377	Confirmation No.: 9994
Appellant:	Ratcliff et al	
Filed:	07/30/2001	
TC/AU:	2644	
Examiner:	Tran	
Docket:	TI-33115	
Cust.No.:	23494	

APPELLANTS' BRIEF

Commissioner for Patents
P.O.Box 1450
Alexandria VA 22313-1450

Sir:

The attached sheets contain the Rule 41.37 items of appellants' brief. The Commissioner is hereby authorized to charge the fee for filing a brief in support of the appeal plus any other necessary fees to the deposit account of Texas Instruments Incorporated, account No. 20-0668.

Respectfully submitted,

/Carlton H. Hoel/

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Rule 41.37(c)(1)(i) Real party of interest

Texas Instruments Incorporated owns the application.

Rule 41.37(c)(1)(ii) Related appeals and interferences

There are no related dispositive appeals or interferences.

Rule 41.37(c)(1)(iii) Status of claims

Claims 1-19 are pending in the application with all claims finally rejected. This appeal involves the finally rejected claims.

Rule 41.37(c)(1)(iv) Status of amendments

There is no amendment to the claims after final rejection.

Rule 41.37(c)(1)(v) Summary of claimed subject matter

The independent claims relate to digital audio processing devices (claims 1, 7, and 13) and methods (claim 18). In particular, application Fig.1 illustrates a claim 1 a device with a plurality of audio inputs (16-21 at left edge of Fig.1), a plurality of audio outputs (22-25, 27, 29 at right edge), a plurality of audio filters (various BQ (biquad filter) blocks in the center), a plurality of audio processing channels (Channel N Processing blocks in right center), and a plurality of multiply switches (various ⊗ symbols in region 11,12 at the left, in region 26 in the center, and in region 13,14 at the right) which allow selective mixing of input signals, filtered signals, and processing channel signals to yield at least one output signal. Figures 2-6 illustrate signal paths for various example multiply switch settings. Application page 6 describes Fig.1.

The device of claim 7 is a “means for” version, and the device of claim 13 focuses on the multiply switches. Claim 18 is a method of using the three pluralities of multiply switches to mix input audio signals, to filter the mixed input audio signals, to mix the filtered audio signals, to channel process the mixed filtered audio signals, and to mix the channel processed audio signals to yield at least one output audio signal.

Rule 41.37(c)(1)(vi) Grounds of rejection to be reviewed on appeal

The grounds of rejection to be reviewed on appeal are:

(1) Claims 1, 6-7, 12-13, and 18 were rejected as unpatentable over the Cowieson reference.

(2) Claims 2-3, 8-9, and 14-15 were rejected as unpatentable over the Cowieson reference in view of the Matheny reference.

(3) Claims 4, 10, and 16 were rejected as unpatentable over the Cowieson reference in view of the Matheny and Tang references.

(4) Claims 1-19 were rejected as unpatentable over the Jacobs reference in view of the Rossmere reference.

Rule 41.37(c)(1)(vii) Arguments

(1) Claims 1, 6-7, 12-13, and 18 were rejected as unpatentable over Cowieson. With regard to independent claim 1, the Examiner cited col. 4, ln. 54-57 for the "processing channels", and cited the summers for the multiply switches.

Appellants reply that the "channels" of col. 4, ln. 54-57 refers to the left and right stereo signals, not to hardware as required by claim 1. Further, the summers of Cowieson do not allow mixing of (i) input signals, (ii) filtered signals, and (iii) channel processed signals as required by claim 1; as Cowieson Figs.1A, 2, and 4 show there are summers between inputs and filters and between filters and outputs, but there are no summers between processing channels and outputs.

With regard to independent claims 7, 13, and 18, the Examiner noted that these claims have limitations similar to those of claim 1.

Appellants agree and make an argument similar to the foregoing argument with regard to claim 1.

(2) Claims 2-3, 8-9, and 14-15 were rejected as unpatentable over Cowieson in view of Matheny.

Appellants rely upon the patentability of parent claims 1, 7, and 13.

(3) Claims 4, 10, and 16 were rejected as unpatentable over Cowieson in view of Matheny and Tang.

Appellants rely upon the patentability of parent claims 1, 7, and 13.

(4) Claims 1-19 were rejected as unpatentable over Jacobs in view of Rossmere. With regard to the independent claim 1, the Examiner cited Jacobs Fig.4, items 64-65 and col. 11, ln. 36-65 for the "processing channels", and Rossmere Fig.3B, items 305, 310 for the plurality of multiply switches.

Appellant's reply that the cited "channels" of Jacobs are signals and not hardware as required by claim 1; see Jacobs col. 11, ln. 57-58. Further, the outputs of the cited filters (Jacobs Fig.4, items 11 at right edge) are directly connected to the outputs and cannot be mixed as required by the hardware of claim 1.

With regard to independent claims 7, 13, and 18, the Examiner noted that these claims have limitations similar to those of claim 1.

Appellants agree and make an argument similar to the foregoing argument with regard to claim 1.

Consequently, the references do not suggest any of the independent claims, and all of the claims are patentable over the references.

Rule 41.37(c)(1)(viii) Claims appendix

1. An audio processing machine comprising:

a plurality of audio inputs;

a plurality of audio outputs;

a plurality of audio filters;

a plurality of audio processing channels; and

a plurality of multiply switches configured to selectively mix the plurality of audio inputs and the plurality of audio outputs such that audio signals passing through the plurality of audio inputs are processed via a plurality of audio filters selected from the plurality of audio filters and a plurality of audio processing channels selected from the plurality of audio processing channels to generate at least one desired audio output signal.

2. The audio processing device according to claim 1 wherein the plurality of multiply switches are comprised of single-cycle multiply switches.

3. The audio processing device according to claim 1 wherein the plurality of multiply switches are comprised of programmable multiply switches.

4. The audio processing device according to claim 3 wherein the programmable multiply switches are reconfigurable on-the-fly.

5. The audio processing device according to claim 1 wherein the multiply switches are further configured to generate a first logic signal to open a conductive path, a second logic signal to close the conductive path, and a third logic signal to open the conductive path while inverting a signal phase associated with an audio signal passing there through.

6. The audio processing device according to claim 1 wherein the plurality of audio filters comprise biquad filters.

7. An audio processing device comprising:

means for receiving a plurality of audio input signals;

means for generating a plurality of audio output signals;

means for filtering the plurality of audio input signals to generate a plurality of filtered audio signals;

means for processing the plurality of filtered audio signals to generate a plurality of processed audio signals; and

a plurality of multiply switches configured to selectively mix a plurality of audio input signals selected from the plurality of audio input signals, a plurality of filtered audio signals selected from the plurality of filtered audio signals and a plurality of processed audio signals selected from the plurality of processed audio signals to generate at least one desired audio output signal.

8. The audio processing device according to claim 7 wherein the plurality of multiply switches are comprised of single-cycle multiply switches.

9. The audio processing device according to claim 7 wherein the plurality of multiply switches are comprised of programmable multiply switches.

10. The audio processing device according to claim 9 wherein the programmable multiply switches are reconfigurable on-the-fly.

11. The audio processing device according to claim 7 wherein the multiply switches are further configured to generate a first logic signal to open a conductive path, a second logic signal to close the conductive path, and a third logic signal to open the conductive path while inverting a signal phase associated with an audio signal passing there through.

12. The audio processing device according to claim 7 wherein the filtering means comprises a plurality of biquad filters.

13. An audio processing device having a plurality of multiply switches operational to selectively mix a plurality of audio input signals, a plurality of filtered audio signals generated therefrom the plurality of audio input signals and a plurality of processed audio signals generated therefrom the plurality of filtered audio signals to generate at least one desired audio output signal.

14. The audio processing device according to claim 13 wherein the plurality of multiply switches comprise single-cycle multiply switches.

15. The audio processing device according to claim 13 wherein the plurality of multiply switches comprise programmable multiply switches.

16. The audio processing device according to claim 15 wherein the programmable multiply switches are reconfigurable on-the-fly.

17. The audio processing device according to claim 13 wherein the multiply switches are configured to generate a first logic signal to open a conductive path, a second logic signal to close the conductive path, and a third logic signal to open the conductive path while inverting a signal phase associated with an audio signal passing there through.

18. A method of processing an audio signal, the method comprising the steps of:

a. configuring a first plurality of multiply switches, a second plurality of multiply switches and a third plurality of multiply switches;

b. mixing a plurality of audio input signals via the first plurality of multiply switches to generate a plurality of mixed audio signals;

c. filtering the plurality of mixed audio signals to generate a first plurality of filtered audio signals;

d. mixing the first plurality of filtered audio signals via the second plurality of multiply switches to generate to generate a second plurality of filtered audio signals;

e. processing the second plurality of filtered audio signals to generate a plurality of processed audio signals; and

f. mixing the plurality of processed audio signals via the third plurality of multiply switches to generate at least one desired audio output signal.

19. The method according to claim 18 further comprising the step of reconfiguring on-the-fly, at least one multiply switch selected from the first, second and third plurality of multiply switches and then repeating steps b-f.

Rule 41.37(c)(1)(ix) Evidence appendix

n/a

Rule 41.37(c)(1)(x) Related proceedings appendix

n/a